CLAIM AMENDMENTS

1-60. (Canceled)

61. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side surface and spaced from the peripheral side surface, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing contacts the chip; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad.

62. (New) The device of claim 61, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

63. (New) The device of claim 62, wherein the first single-piece housing portion contacts the lower and outer side surfaces.

64. (New) The device of claim 62, wherein the first single-piece housing portion is spaced from the upper surface.

65. (New) The device of claim 62, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface.

66. (New) The device of claim 62, wherein the second single-piece housing portion is farther from the top surface than the lower surface is from the top surface.

67. (New) The device of claim 61, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

68. (New) The device of claim 61, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

69. (New) The device of claim 61, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

70. (New) The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

71. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side

surface and spaced from the peripheral side surface, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing covers the lower surface and contacts the chip; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad, wherein an electrically conductive path between and in contact with the lead and the pad is devoid of a wire bond.

72. (New) The device of claim 71, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

73. (New) The device of claim 72, wherein the first single-piece housing portion contacts the lower and outer side surfaces.

74. (New) The device of claim 72, wherein the first single-piece housing portion is spaced from the upper surface.

75. (New) The device of claim 72, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface.

76. (New) The device of claim 72, wherein the second single-piece housing portion is farther from the top surface than the lower surface is from the top surface.

77. (New) The device of claim 71, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

78. (New) The device of claim 71, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

79. (New) The device of claim 71, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

80. (New) The device of claim 71, wherein the device is devoid of wire bonds, TAB leads and solder joints.

81. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side surface and spaced from the peripheral side surface, the peripheral portion is integral with the peripheral and inner side surfaces and non-integral with the central portion, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing contacts and covers the lower surface; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad, wherein an electrically conductive path between and in contact with the lead and the pad is devoid of a wire bond.

82. (New) The device of claim 81, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

83. (New) The device of claim 82, wherein the first single-piece housing portion contacts the lower and outer side surfaces and is spaced from the upper surface.

84. (New) The device of claim 82, wherein the first single-piece housing portion contacts the entire lower surface.

85. (New) The device of claim 82, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface and is farther from the top surface than the lower surface is from the top surface.

86. (New) The device of claim 82, wherein the second single-piece housing portion contacts the electrically conductive path.

87. (New) The device of claim 81, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

88. (New) The device of claim 81, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

89. (New) The device of claim 81, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

90. (New) The device of claim 81, wherein the device is devoid of wire bonds, TAB leads and solder joints.

91. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side surface and spaced from the peripheral side surface, the peripheral portion is integral with the peripheral and inner side surfaces and non-integral with the central portion, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing contacts and covers the lower surface; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad, wherein an electrically conductive path between and in contact with the lead and the pad is devoid of a wire bond, and the lead and the electrically conductive path are no closer to the top surface than the upper surface is to the top surface.

92. (New) The device of claim 91, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral portion

of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

93. (New) The device of claim 92, wherein the first single-piece housing portion contacts the lower and outer side surfaces and is spaced from the upper surface.

94. (New) The device of claim 92, wherein the first single-piece housing portion contacts the entire lower surface.

95. (New) The device of claim 92, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface and is farther from the top surface than the lower surface is from the top surface.

96. (New) The device of claim 92, wherein the second single-piece housing portion contacts the electrically conductive path.

97. (New) The device of claim 91, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

98. (New) The device of claim 91, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

99. (New) The device of claim 91, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

100. (New) The device of claim 91, wherein the device is devoid of wire bonds, TAB leads and solder joints.

101. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side surface and spaced from the peripheral side surface, the peripheral portion is integral with the peripheral and inner side surfaces and non-integral with the central portion, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing contacts and covers the lower and outer side surfaces; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, and an electrically conductive path between and in contact with the lead and the pad is devoid of a wire bond.

102. (New) The device of claim 101, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

103. (New) The device of claim 102, wherein the first single-piece housing portion contacts the lower and outer side surfaces and is spaced from the upper surface.

104. (New) The device of claim 102, wherein the first single-piece housing portion contacts the entire lower surface.

105. (New) The device of claim 102, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface and is farther from the top surface than the lower surface is from the top surface.

106. (New) The device of claim 102, wherein the second single-piece housing portion contacts the electrically conductive path.

107. (New) The device of claim 101, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

108. (New) The device of claim 101, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

109. (New) The device of claim 101, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

110. (New) The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

111. (New) A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, a peripheral side surface between the top and bottom surfaces, and an inner side surface opposite the peripheral side surface, wherein the bottom surface includes a peripheral portion adjacent to the peripheral and inner side surfaces and a central portion within the peripheral portion adjacent to the inner side surface and spaced from the peripheral side surface, the peripheral portion is integral with the peripheral and inner side surfaces and non-integral with the central portion, the peripheral portion protrudes downwardly from the central portion, and the top and bottom surfaces, peripheral and inner side surfaces and peripheral and central portions are exposed;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface, a lower surface and an outer side surface between the upper and lower surfaces, the upper surface includes a conductive pad, faces towards the central portion and faces away from the top surface, and the insulative housing contacts and covers the lower and outer side surfaces; and

a lead that protrudes laterally from and extends through the peripheral side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, an electrically conductive path between and in contact with the lead and the pad is devoid of a wire bond, and the lead and the electrically conductive path are no closer to the top surface than the upper surface is to the top surface.

112. (New) The device of claim 111, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion, the first single-piece housing portion provides the top surface, the peripheral and inner side surfaces and the peripheral

portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

113. (New) The device of claim 112, wherein the first single-piece housing portion contacts the lower and outer side surfaces and is spaced from the upper surface.

114. (New) The device of claim 112, wherein the first single-piece housing portion contacts the entire lower surface.

115. (New) The device of claim 112, wherein the second single-piece housing portion is no closer to the top surface than the upper surface is to the top surface and is farther from the top surface than the lower surface is from the top surface.

116. (New) The device of claim 112, wherein the second single-piece housing portion contacts the electrically conductive path.

117. (New) The device of claim 111, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

118. (New) The device of claim 111, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

119. (New) The device of claim 111, wherein the device includes a plurality of leads, the chip includes a plurality of pads, each of the leads is electrically connected to one of the pads inside the insulative housing and outside the chip, and the leads are arranged as TSOP leads that protrude laterally from and extend through the peripheral side surface and an opposing peripheral side surface of the insulative housing.

120. (New) The device of claim 111, wherein the device is devoid of wire bonds, TAB leads and solder joints.